Comparison of Si SJMOS and SiC MOSFET for Single Phase PFC Application

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***Abstract*—Silicon superjunction MOSFET (Si SJMOS) with SiC Schottky diode is a popular choice in single-phase dual-boost PFC converter applications due to their lower cost, standard gate driving voltage, and high reliability. SiC Schottky barrier diode (SBD) can mitigate the issue of poor reverse recovery of the body diode of Si SJMOS and improve the converter's efficiency. SiC MOSFETs are now available in the voltage range of 600-650V, where they can be used as an alternative to the Si SJMOS. It is generally believed that using SiC MOSFET in place of Si SJMOS will increase the converter's efficiency. However, SiC MOSFET in this voltage range (600-650V) has a similar on-state performance to Si SJMOS. On the other hand, SiC MOSFET is expensive when compared with Si SJMOS. Also, being a new device, the reliability data for SiC MOSFETs from the field is not available. This work presents a comparative study of the switching dynamics of similarly rated SiC MOSFET and Si SJMOS, where SiC SBD is used as a free-wheeling diode. Two sets of 650V SiC MOSFET and Si SJMOS of different current ratings are considered for comparison. The experiments are conducted for a range of gate resistance and operating currents.**

***Index Terms*—Silicon superjunction MOSFETs, CoolMOS, Silicon carbide MOSFETs, Schottky Diode, PFC**

I. Introduction

Single-phase power factor correction (PFC) converter is widely used as the active front-end (AFE) in many applications such as electric vehicle (EV) onboard charger, telecom and data center power supply, etc. 600-650V devices are suitable for these applications. Si superjunction MOSFETs (SJMOS) have been dominating the market in this voltage segment of 600-650V and are used extensively in commercial designs. Though Si is a popular choice, reverse recovery of the free-wheeling diode is one of the major concerns in Si-based designs [1]. It reduces efficiency and may lead to EMI related issues [2]. To mitigate the problems related to reverse recovery in Si-based designs, dual-boost PFC as shown in Fig. 1 can be a good alternative where Si P-i-N diodes (D_1 and D_2) are replaced with majority carrier SiC Schottky diode (SBD). Please note that SiC SBDs are also available in the range of 600-650V with better conduction loss performance and zero reverse recovery [3]. This configuration will be beneficial in achieving higher efficiency and power density for designs where the power flow is unidirectional [4].

However, the recent emergence of the wide bandgap devices such as gallium nitride (GaN) and silicon carbide (SiC) power

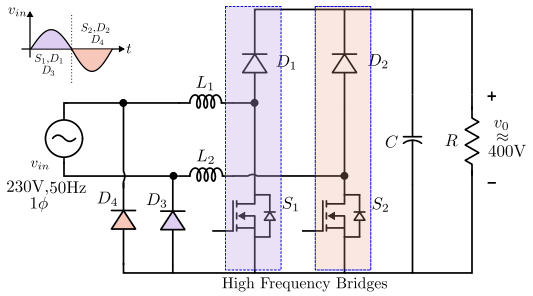


Fig. 1. Dual Boost PFC

semiconductor devices have challenged the dominance of the Si SJMOS. GaN transistors have the features like fast switching speed, low conduction and switching losses, and zero reverse recovery. However, slow adoption of these devices is reported due to their limited reliability characteristics such as threshold voltage instability, dynamic on-state resistance, etc [5]–[8]. Also, the low overdrive safety margin (1-4 V) of these transistors requires special gate drive circuit design considerations and makes them more susceptible to failure [9]. Conversely, SiC technology has started to mature, and they are more suitable for commercial designs.

SiC transistors can be segregated into junction field-effect transistors (JFETs) and metal-oxide-semiconductor field-effect transistors (MOSFETs). SiC JFETs are normally-on devices and usually not preferred in the power electronic converters due to safety reasons [10]. Also, these devices are not available commercially. On the other hand, SiC MOSFETs are normally-off devices and have been commercialized. Hence, in this work, Si SJMOS and SiC MOSFET are considered for comparison.

The comparison of Si and SiC devices has earlier been conducted in [11]–[14]. Among these, [11], [12] present a comparison of Si SJMOS and SiC MOSFET with different current and voltage ratings. In both cases, SiC MOSFET is 1200V rated, whereas Si SJMOS of lower voltage rating is used (600V rated in [11] and 500V rated in [12]). [11] compares the hard switching loss, whereas soft switching loss was compared in [12]. However, the conclusions of these works cannot be used for the single-phase PFC based application discussed previously, as the voltage ratings of the

devices are not similar. In [13], [14], devices of the same voltage ratings (600-650V) are used for comparison. Among them, [14] considers devices of different current ratings (35A for Si SJMOS and 118A for SiC MOSFET), and the switching power loss is compared for a buck converter configuration for three different load currents and four different frequencies of operation. However, this comparison can not be justified as the current ratings of the devices are hugely different (also the on-state resistance). [13] also considers the devices of similar current ratings. However, the switching transition waveforms are presented only for one operating condition, and comparison results are not extensive. Also, the SiC SBD used for this application is 1200V rated, which is not a practical choice for a 400V application.

From the above discussion, it can be concluded that there is still a lack of comparative study on the switching dynamics of Si SJMOS and SiC MOSFET in single-phase dual-boost PFC application where SiC SBD of similar voltage rating is used as a freewheeling diode. This work addresses this gap and presents a comparison of the switching loss performance of similarly rated Si SJMOS and SiC MOSFET. SiC SBD of similar voltage rating (650V) is used as a freewheeling diode. Two separate Si SJMOS and SiC MOSFET pairs with different current ratings (30 and 60A) are considered for comparison. The selected device pairs have similar on-state resistances and hence similar conduction performance. Double pulse test based experiments are conducted for a range of gate resistance and operating currents. Similar gate and power circuit layouts are maintained for both Si SJMOS and SiC MOSFET for switching transient comparison. The switching transition time, switching loss, (dv/dt), (di/dt) are compared for both the devices and a qualitative discussion is also presented.

This paper is arranged in the following order. Description of the experimental setup and selected devices used for this comparison study are given in section II. Section III presents the comparison of the switching losses, times, and (dv/dt) and (di/dt) rates for Si SJMOS and SiC MOSFET for a range of operating conditions. Finally, section IV concludes the paper.

II. Experimental Setup and Device Selection

In this section, details about the experiment, setup and the devices used for the comparison of the switching dynamics of Si SJMOS and SiC MOSFETs are presented.

A. Double Pulse Test Experiment

Double pulse test (DPT) is an experimental method of capturing the switching dynamics of a power semiconductor device. A buck-chopper configuration with an output inductive load is used in the DPT, as shown in Fig. 2(a). Two pulses of different widths are applied to the power device. During the first pulse, current in the output inductor builds up to the required current level I_0. The device is then switched off and on to obtain the turn-off and turn-on switching transitions as shown in Fig. 2(b). Switching losses are incurred during these transitions due to the non-zero product of the current and voltage.

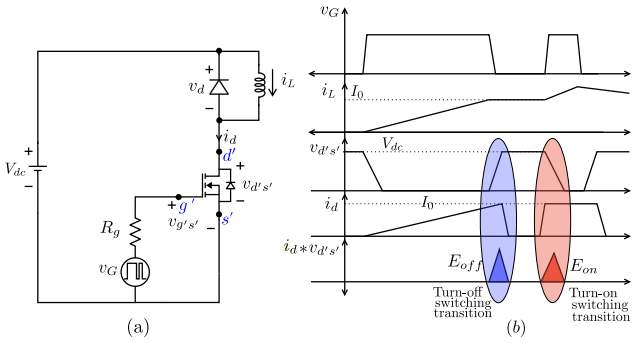


Fig. 2. Schematic of the DPT and idealised waveforms

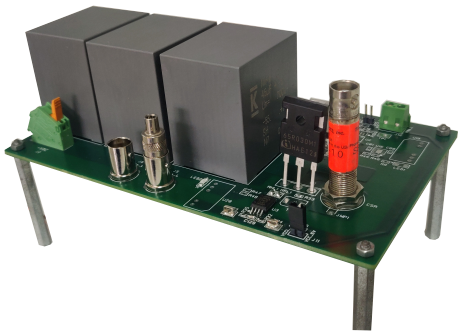


Fig. 3. DPT setup for comapring the switching dynamics of Si SJMOS and SiC MOSEFET

Fig. 3 shows the DPT experimental setup used for this comparison study. A custom-made air-cored inductor of value $L_0 = 150\mu H$ is connected as the inductive load. Three $45\mu F$ film capacitors decouple the input power supply and form the dc bus capacitance. Four sets of $0.1\mu F$ SMD transient capacitors in series with 4Ω resistors are used to reduce the power loop inductance and to provide damping during the switching transitions.

B. Device Selection

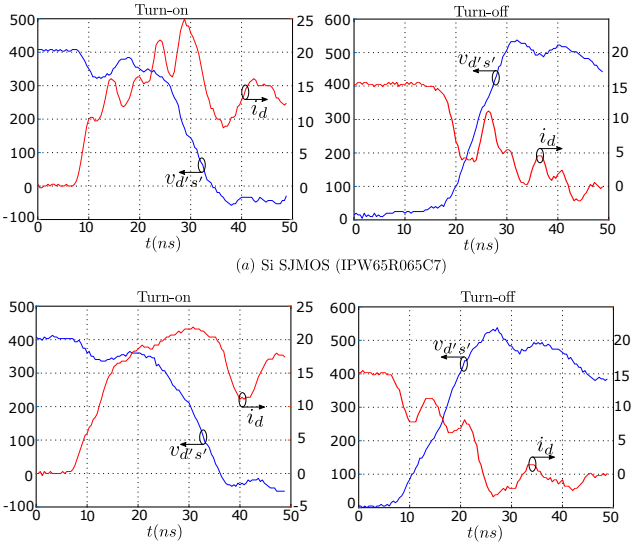
To obtain a like-for-like comparison, Si SJMOS and SiC MOSFET with similar voltage and current ratings, and on-state resistances are selected. This comparison is presented at two different current levels ($\approx 30A$ and $\approx 60A$) to cater to the entire power level (2-5 kW) for a single-phase converter. The key features of the devices are listed in Table I. While SiC MOSFETs support higher temperature operation, and lower dependence of the on-state resistance $R_{ds(on)}$ on the temperature, its thermal resistance $R_{th(jc)}$ is comparatively greater than the Si SJMOS. Also, SiC MOSFETs have smaller gate charge Q_g, and hence it will incur smaller power dissipation in the gate drive circuit as compared to the Si SJMOS. However, Si SJMOS are cheaper than the SiC MOSFETs. Also, the output charge Q_{oss} of Si SJMOS is significantly higher than that of SiC MOSFET. SiC SBD are majority carrier device and possesses only a small amount of capacitive charge Q_c due to its reverse-biased depletion capacitance, and it increases with the current rating of the SiC SBD.

TABLE I
KEY FEATURES OF THE SELECTED DEVICES

	Part No.	Technology	Voltage Rating (V)	Current Rating (A)		$T_{J(max)}$ $(°C)$	$R_{ds(on)}$ $(m\Omega)$		$R_{th(jc)}$ $(°C/W)$	Q_g (nC)	$Q_{oss}(Q_c)$ (nC)	Gate Voltage (V)	Price (INR)
				$25°C$	$100°C$		$25°C$	$T_{J(max)}$					
Pair P_1	IPW65R065C7	Si SJMOS	650	33	21	150	58	138	0.73	64	444	+15/0	934.12
	IMW65R057M1H	SiC MOSFET	650	35	25	175	57	80	1.13	28	64.8	+18/0	1208.42
	C6D10065A	SiC SBD	650	37	23	175	-	-	1.38	-	34	-	482.77
Pair P_2	IPW60R031CFD7	Si SJMOS	600	63	40	150	26	59	0.45	141	840.4	+15/0	1160.18
	IMW65R030M1H	SiC MOSFET	650	58	41	175	30	42	0.76	48	113.6	+18/0	1789.31
	CVFD20065A	SiC SBD	650	57	40	175	-	-	0.8	-	62	-	843.64

TABLE II
KEY GATE DRIVER PARAMETERS

External Gate resistance (Ω)	Driver on resistance (Ω)	Driver off resistance (Ω)	CMTI (V/ns)	Cio (pF)
5,10	0.45	0.35	200	0.9



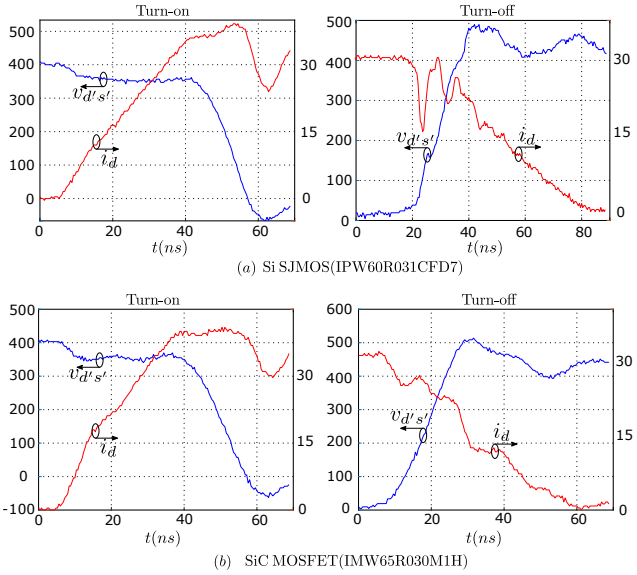
(a) Si SJMOS (IPW65R065C7)

(b) SiC MOSFET (IMW65R057M1H)

Fig. 4. Experimentally obtained switching dynamics of Si SJMOS and SiC MOSFET for pair P_1 [$V_{dc} = 400V, R_{g(ext)} = 5\Omega$ and $I_0 = 15A$]

C. Gate drive cicruit

Standard gate drive voltage $+15/0$V is used for Si SJMOS, and SiC MOSFET is driven with their recomended $+18/0$V voltage levels. This ensures the operation of the devices at their recommended on-state resistances and at similar conduction loss. Isolated gate driver 1ED3123MU12H from Infineon technologies is used for driving the power devices as it has the best common-mode transient immunity (CMTI) rating of $200V/ns$ and low input-output coupling capacitance among the commercially available gate drivers. Moreover, it also features separate sourcing and sinking current paths for individual control of the turn-on and turn-off transition speed. Key parameters of the gate driver are listed in Table II.



(a) Si SJMOS(IPW60R031CFD7)

(b) SiC MOSFET(IMW65R030M1H)

Fig. 5. Experimentally obtained switching dynamics of Si SJMOS and SiC MOSFET for pair P_2 [$V_{dc} = 400V, R_{g(ext)} = 5\Omega$ and $I_0 = 30A$]

D. Test conditions and Measurement

The DPT experiments are conducted for a dc bus voltage of 400V and for two values of external gate resistances $R_{g(ext)} = 5, 10\Omega$. The experimental measurements are done for five values of load current (5-25 A in steps of 5A) for pair P_1 and (10-50A in steps of 10A) for pair P_2. This comprises a total of 20 operating conditions. The experiments were conducted at room temperature of about $25°C$. The drain-source voltage $v_{d's'(t)}$, gate-source voltage $v_{g's'(t)}$ and drain current $i_d(t)$ are important waveforms for this comparison study (see Fig. 2). These signals are captured in a 1 GHz mixed-signal oscilloscope (MDO2104) from Tektronix. Passive voltage probe TPP1000 of 1 GHz bandwidth is used for measuring $v_{g's'(t)}$, and single-ended high-voltage probe P5100A with 500 MHZ bandwidth is used for $v_{d's'(t)}$ measurement. Coaxial current shunt resistor (CSR) SSDN-10 from T&M Research is used for measuring $i_d(t)$ as it has low parasitic inductance $\approx 4nH$. A shielded BNC cable is used for connecting the CSR with the oscilloscope. Before the experiment, the propagation delay of the voltage and current probes were matched using a deskew and calibration fixture 067-1686-00 from Tektronix.

Once the signals are captured in the oscilloscope, it is

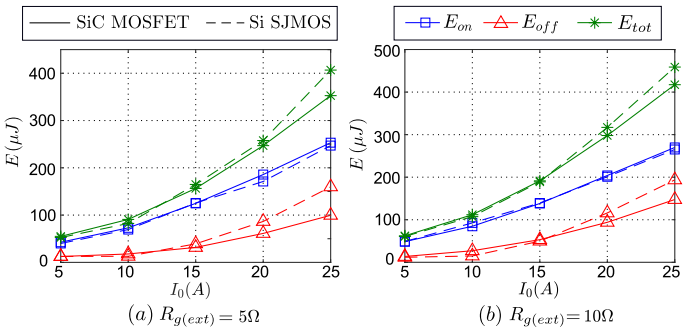


Fig. 6. Comparison of Switching Loss of Si SJMOS and SiC MOSFET for Pair 1 (a) $R_{g(ext)} = 5\Omega$ (b) $R_{g(ext)} = 10\Omega$; E_{on} = Turn-on switching energy loss, E_{off} = Turn-off switching energy loss, and E_{tot} = E_{on}+E_{off}

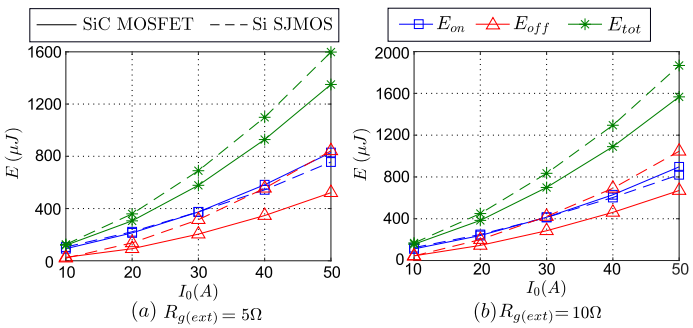


Fig. 7. Comparison of Switching Loss of Si SJMOS and SiC MOSFET for Pair 2 (a) $R_{g(ext)} = 5\Omega$ (b) $R_{g(ext)} = 10\Omega$; E_{on} = Turn-on switching energy loss, E_{off} = Turn-off switching energy loss, and E_{tot} = E_{on}+E_{off}

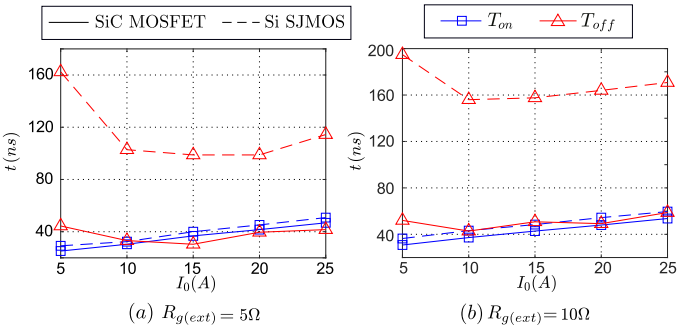


Fig. 8. Comparison of Switching times of Si SJMOS and SiC MOSFET for Pair 1 (a) $R_{g(ext)} = 5\Omega$ (b) $R_{g(ext)} = 10\Omega$; T_{on} = Turn-on switching transition time, T_{off} = Turn-off switching transition time

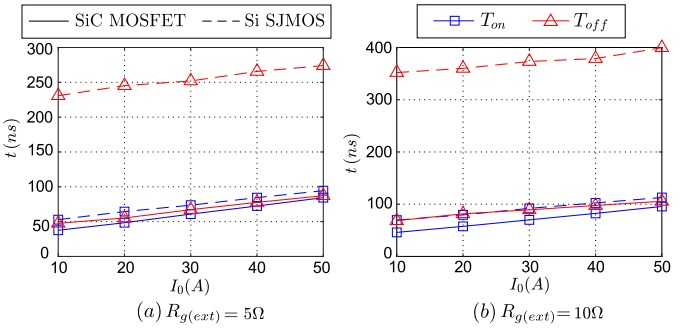


Fig. 9. Comparison of Switching times of Si SJMOS and SiC MOSFET for Pair 2 (a) $R_{g(ext)} = 5\Omega$ (b) $R_{g(ext)} = 10\Omega$; T_{on} = Turn-on switching transition time, T_{off} = Turn-off switching transition time

processed in MATLAB to obtain switching loss, switching transitions times, and (dv/dt) and (di/dt) rates for the comparison study.

III. Results and Discussion

In this section, important switching dynamics-related quantities such as switching loss, switching times, and (dv/dt) and (di/dt) rates of Si SJMOS are compared with that of SiC MOSFETs for the two device pairs P_1 and P_2. Switching dynamics for both pairs are captured experimentally using the double pulse test setup as described in the previous section for a range of load currents and external gate resistances. Fig. 4 shows the experimentally obtained switching dynamics for pair P_1 for one operating condition [$V_{dc} = 400V, R_{g(ext)} = 5\Omega$ and $I_0 = 15A$]. Similarly, the switching dynamics obtained for the pair P_2 is shown in Fig. 5 for the operating condition [$V_{dc} = 400V, R_{g(ext)} = 5\Omega$ and $I_0 = 30A$]. These waveforms are then processed to obtain losses, times, and (dv/dt) and (di/dt) rates. The comparison results are discussed in the following subsections.

A. Comparison of switching losses

In Fig. 6, experimentally obtained switching energy losses of both Si SJMOS and SiC MOSFET for the pair P_1 are plotted as a function of the load current I_0 for two values of external gate resistances, $R_{g(ext)} = 5\Omega$ and $R_{g(ext)} = 10\Omega$. The experiments were conducted at the dc bus voltage of 400V. Fig. 7 shows a similar plot for the MOSFETs of the pair P_2.

The following important observations can be obtained from these plots.

- Turn-on switching energy loss of both Si SJMOS and SiC MOSFET are similar, with slightly smaller losses for Si SJMOS. This observation is true for both the pairs of devices and for majority of the operating conditions shown.
- Turn-off switching energy loss of Si SJMOS is slightly greater than SiC MOSFET, and the difference grows with the value of load current. This observation is even more dominant for the high-current devices.
- The total switching loss (E_{tot}) of Si SJMOS is slightly higher than SiC MOSFET due to the higher turn-off loss of Si SJMOS.

However, in a practical converter, devices will be operated close to or below 50% of the rated current to account for both conduction and switching loss. And it can be observed that for the above load conditions switching loss of Si SJMOS and SiC MOSFET are very similar to one another for both high and low current device pairs.

B. Comparison of switching times

Fig. 8 compares the turn-on and turn-off switching times of the low current (pair 1) Si SJMOS and SiC MOSFET for two values of $R_{g(ext)} = 5, 10\Omega$. A similar comparison for the

TABLE III
COMPARISON OF dv/dt FOR SI SJMOS AND SIC MOSFETS (PAIR 1)

$R_{g(ext)}$ (Ω)	I_0 (A)	$\left(\frac{dv_{ds}}{dt}\right)_{on}$ (Vns)		$\left(\frac{dv_{ds}}{dt}\right)_{off}$ (V/ns)	
		Si SJMOS	SiC MOSFET	Si SJMOS	SiC MOSFET
5Ω	5	43.71	35.29	18.75	16.8
	10	30.6	29.71	34.59	28.57
	15	37.5	28.36	39.75	31.59
	20	35.29	28.37	40.8	33.33
	25	39	26.73	40.8	36.71
10Ω	5	36.71	30	20.4	17.294
	10	32.67	25	34.59	25
	15	36.75	25.57	30.95	28.36
	20	33.47	24.48	30.6	28.57
	25	38.25	25.5	31.2	28.36

TABLE IV
COMPARISON OF dv/dt FOR SI SJMOS AND SIC MOSFETS (PAIR 2)

$R_{g(ext)}$ (Ω)	I_0 (A)	$\left(\frac{dv_{ds}}{dt}\right)_{on}$ (Vns)		$\left(\frac{dv_{ds}}{dt}\right)_{off}$ (V/ns)	
		Si SJMOS	SiC MOSFET	Si SJMOS	SiC MOSFET
5Ω	10	25.6	24.75	25.5	20.4
	20	28.29	23.25	22	25.5
	30	27.2	22.67	24	25.5
	40	28	20.84	22.11	27.2
	50	27.2	19.8	20.67	30
10Ω	10	23.29	19.42	22	14.89
	20	24.71	20.57	20	18.29
	30	23.29	18	19.43	19.64
	40	24	16.5	19.43	20
	50	24.75	18	19.43	21

TABLE V
COMPARISON OF di/dt FOR SI SJMOS AND SIC MOSFETS (PAIR 1)

$R_{g(ext)}$ (Ω)	I_0 (A)	$\left(\frac{di}{dt}\right)_{on}$ (A/ns)		$\left(\frac{di}{dt}\right)_{off}$ (A/ns)	
		Si SJMOS	SiC MOSFET	Si SJMOS	SiC MOSFET
5Ω	5	3.844	2.108	0.281	0.347
	10	3.398	1.916	1.083	1.15
	15	2.422	1.896	0.521	1.772
	20	1.249	1.25	0.299	0.769
	25	1.42	1.185	0.337	0.808
10Ω	5	1.84	1.198	0.319	0.347
	10	1.428	1.374	1.25	0.958
	15	0.97	1.112	0.5	0.619
	20	1.005	1.029	0.433	0.794
	25	0.899	1.004	0.486	0.694

TABLE VI
COMPARISON OF di/dt FOR SI SJMOS AND SIC MOSFETS (PAIR 2)

$R_{g(ext)}$ (Ω)	I_0 (A)	$\left(\frac{di}{dt}\right)_{on}$ (A/ns)		$\left(\frac{di}{dt}\right)_{off}$ (A/ns)	
		Si SJMOS	SiC MOSFET	Si SJMOS	SiC MOSFET
5Ω	10	1.3432	1.807	0.357	0.8211
	20	1.024	1.228	0.399	0.639
	30	0.984	1.103	0.548	0.638
	40	0.965	1.011	0.566	0.681
	50	0.955	0.938	0.557	0.692
10Ω	10	0.807	1.157	0.369	0.722
	20	0.862	0.977	0.451	0.536
	30	0.876	0.941	0.464	0.562
	40	0.887	0.905	0.478	0.616
	50	0.885	0.861	0.487	0.658

high-current devices (pair 2) are shown in Fig. 9. It can be observed that while the turn-on switching transition times of Si SJMOS and SiC MOSFET are similar, Si SJMOS has s considerably higher turn-off time. This is true for both low- and high-current device pairs and for the range of operating conditions. As a result, the total switching time of Si SJMOS is higher than SiC MOSFET.

Higher turn-off transition time has a direct consequence on the deadtime requirement for the proper operation of the converter. From Fig. 8 and Fig. 9, it can be observed Si SJMOS-based converter would require about 2-3 times the deadtime as that of the SiC MOSFET-based converter.

C. (dv/dt) Comparison

Experimentally obtained rate of change of drain-source voltage (dv/dt) of both Si SJMOS and SiC MOSFET for pair P_1 are tabulated as a function of the load current I_0 for $R_{g(ext)} = 5\Omega$ and $R_{g(ext)} = 10\Omega$ in Table III. Similar results are also given for the pair P_2 in Table IV. It can be observed that the turn-on (dv/dt) $((dv/dt)_{on})$ of both Si SJMOS and SiC MOSFET remains almost invariant with I_0 for a given value of $R_{g(ext)}$. It is worthwhile to note that the $(dv/dt)_{on}$ of Si SJMOS is slightly higher than the SiC MOSFET. Similar to $(dv/dt)_{on}$, turn-off (dv/dt) $((dv/dt)_{off})$ of Si SJMOS is also slightly higher than SiC MOSFET. Unlike $(dv/dt)_{on}$, $(dv/dt)_{off}$reduces for small values of I_0. However, it becomes almost constant for high I_0 values. Kindly note that (dv/dt) of Si SJMOS and SiC MOSFET during both the turn-on and the turn-off switching transitions are of the similar order due to the similar order of the reverse transfer and the output capacitances. This directly affects the performance of the common-mode filter.

D. (di/dt) Comparison

Similar to (dv/dt), experimentally obtained (di/dt) for both the device pairs P_1 and P_2 are listed in Table V and Table VI, respectively, for the same operating conditions. It can be observed that turn on (di/dt) $((di/dt)_{on})$ of both Si SJMOS and SiC MOSFET are of similar order for most of the operating conditions except few low I_0 values. It is also observed that $(di/dt)_{on}$ has a weak dependence on the load current I_0.Also, $(di/dt)_{on}$ has weak dependence on $R_{g(ext)}$. This may be due to the impact of common source inductance during the current rise period of switching transient. Unlike $(di/dt)_{on}$, $(di/dt)_{off}$ of Si SJMOS is small compared to the $(di/dt)_{off}$ of SiC MOSFET for both the device pairs P_1 and P_2 for most of the operating conditions. In general, $(di/dt)_{off}$ of both Si SJMOS and SiC MOSFET are found to be small compared to $(di/dt)_{on}$.

IV. CONCLUSION

In this work, an experimental investigation into the switching dynamics comparison of Si SJMOS and SiC MOSFET is presented. A buck-chopper circuit with SiC SBD as the

freewheeling diode is selected for this comparison which is applicable to PFC converters such as the dual-boost PFC. Two sets of 650V SiC MOSFET and Si SJMOS of different current ratings (30 and 60A) are considered for comparison. The experiments are conducted at the dc bus voltage of 400V and for a range of operating currents and two values of external gate resistances. Switching transition times, switching loss, and dv/dt and (di/dt) are compared for the device pairs, and important observations are discussed.

Total switching loss of Si SJMOS is found to be slightly higher than the SiC MOSFET due to higher turn-off switching loss of Si SJMOS. However, for normal converter operation, load currents are usually less than 50% of the rated current of the devices, and in these load current ranges, switching loss performance of both the devices are very similar. Similar to the losses, the turn-off switching time of Si SJMOS is also higher than SiC MOSFET due to the high value of its internal input capacitance. As a result, Si SJMOS based converter would require a higher deadtime than SiC MOSFET based converter. Also, both devices have (dv/dt) and (di/dt) of the similar order.

Hence, from this comparative study, it can be concluded that both Si SJMOS and SiC MOSFET have similar switching loss performance, and both can be equally selected for the PFC application. However, lower prices and high reliability due to decades of field operation as compared to SiC MOSFET, Si SJMOS are still a strong competitor in the PFC applications where SiC Schottky diodes are used as the synchronous device such as the dual-boost PFC, etc.

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